REMARKS

Claims 1-13 and 21 are pending. Claim 1 is amended hereby. A marked-up version showing the changes made to claim 1 is attached hereto as **"Version with markings to show changes made."**

As a preliminary matter, an Information Disclosure Statement was filed on May 24, 2002. The Examiner is requested to acknowledge consideration of the references cited therein with the next communication.

Claims 1-13 and 21 were rejected under 35 USC § 112, second paragraph, as being indefinite. Amended claim 1 no longer refers to a trench. As such, the rejection is moot.

Claims 1-13 and 21 were rejected under 35 USC § 102(e) as being anticipated by ***Mizuhara et al.*** or ***Watanabe et al.*** Favorable reconsideration of this rejection is earnestly solicited.

Claim 1 has been amended to specify that the first insulation layer is formed on a flat underlying face over a substrate. The cited art fails to teach or suggest the features of amended claim 1.

More specifically, the first insulation layer defined in amended claim 1 is not formed on structural elements having concave and convex portions, but instead is formed on a flat underlying face over a substrate. Accordingly, the film thickness of the first insulation layer becomes uniform, and modification by impurity introduction is effected uniformly (see page 9, line 32 through page 10, line 2 of the specification). Thus, microfabrication of a semiconductor device having extremely

high dimensional accuracy is enabled, avoiding various troubles associated with miniaturization.

In contrast thereto, ***Mizuhara et al.*** provides an insulation layer into which impurities are introduced after the formation of a structure with concave and convex portions as shown in Figs. 4-6. Similarly, ***Watanabe et al.*** provides an uneven underlying layer as illustrated in Figs. 4 and 5 thereof. An insulation layer formed on such an underlying layer will be uneven in thickness. As such, a minaturized semiconductor device of high dimensional accuracy cannot be obtained as in the present invention.

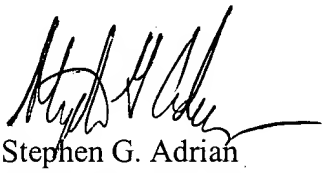
For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicants' undersigned attorney.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully Submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



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Enclosure: Version with markings to show changes made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/320,271

IN THE CLAIMS:

Claim 1 has been amended as follows:

1. **(Four Times Amended)** A fabrication method of a semiconductor device comprising the steps of:

forming a first insulation layer on a flat underlying face over a substrate,

introducing impurities into said first insulation layer,

[forming, in said first insulation layer, a trench extending in a line,] and

embedding and forming a first conductive layer in said [trench extending linearly] first insulation layer.